AMENDMENTS TO THE SPECIFICATION

Please replace paragraphs **[0060]** through **[0062]** with the following amended paragraphs:

[0060] The principles of the invention may be implemented in different ways. The data may be processed in parallel as shown in Figs. 10 and 12, or stored and processed serially as shown in Figs. 9 and 11. In the implementation of Fig. 9, a single PLL with inner block decoder ~~910~~ 710 receives the input modulated signal at successive different frequencies. It first processes the signal for a first frequency using multiple phase estimates. The signal is processed at the first frequency for a number of times equal to the number of phase estimates. PLL ~~910~~ 710 then processes the input modulated signal for a second frequency using the same multiple phase estimates. The signal is processed at the second frequency for the same number of times as the first frequency. This is repeated until the signal is processed for all combinations of the frequencies and phase estimates. The signal is stored temporarily to allow multiple serial processings. For example, if there are two different frequencies and four different initial phase estimates, then there will be eight (2 x 4) different output results from PLL ~~910~~ 710. Selection Circuit ~~920~~ 720 receives all of the outputs in sequence and selects the output having the best correlation metric to be passed onto an outer block decoder, such as a Reed-Solomon block decoder (not shown in Fig. 9).

[0061] In the implementation of Fig. 10, there are multiple PLLs ~~1001-1~~ 801-1 to ~~1001-n~~ 801-n, each with a respective inner block decoder. Each PLL receives the input signal using a single frequency and a single initial phase estimate. In this implementation, the number of PLLs is equal to the number of possible combinations of frequency and initial phase estimates. Each PLL has a unique combination of frequency and initial phase estimate. Selection circuit ~~1020~~ 820 receives the outputs of each one of PLLs ~~1001-1~~ 801-1 to 801-n and selects the output having the best correlation metric to be passed onto an outer block decoder, such as a Reed-Solomon block decoder (not shown in Fig. 10).

[0062] In the implementation of Fig. 11, the input signal is serially processed with multiple initial phase/frequency estimates in a single PLL ~~1110~~ 910 as described with reference to Fig. 9. However, the outputs from PLL ~~1110~~ 910 are provided directly to a Reed-Solomon block decoder ~~1120~~ 920 for decoding of codeword errors. Selection circuit ~~1130~~ 930 receives the serial outputs from Reed-Solomon block decoder ~~1120~~ 920 and selects the output for the initial phase/frequency estimate which corrects all of the errors/erasures in the codewords. In the implementation of Fig. 12, the input signal is processed in parallel in multiple PLLs ~~1201-1~~ 1001-1 to ~~1201-n~~ 1001-n as described above with reference to Fig. 11. However, the outputs from PLLs ~~1201-1~~ 1001-1 to ~~1201-n~~ 1001-n are provided directly to respective Reed-Solomon block decoders ~~1210-1~~ 1010-1 to ~~1210-n~~ 1010-n for decoding of codeword errors. Selection circuit ~~1220~~ 1020 receives the outputs from all of the Reed-Solomon block decoders ~~1210-1~~ 1010-1 to ~~1210-n~~ 1010-n, and selects the output for the initial phase/frequency estimate which corrects all of the errors/erasures in the codewords. If none of the outputs are correct, then the data can be discarded as usual.